EE/CprE/SE 491 WEEKLY REPORT 10

Date: ***Apr 16th, 2023 – Apr 30th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

In this past week, we made more progress toward the development of our components and getting them through the process flow. We were able to create a correct layout for the 1-bit ADC and get that layout to pass an LVS check. Along with getting more of our components through the process flow, we were finally able to get a simulation of the ReRAM device that was provided in the Skywater 130 nm pdk. We were able to observe the switching behavior that is inherent in the device. However, after showing the waveforms to our advisor, we realized that the ReRAM model may not be very good. Since this is the only thing we have to go off of, we will continue with it, but it is something important to keep in mind.

Past week accomplishments

- Joshua Thater
    - Rebuilt Xyce with the correct configurations
    - Simulated ReRAM and observed the expected switching behavior (although it may not be a perfect model)
    - Tried to figure out how to simulate other devices with the ReRAM device
- Aiden Petersen
    - Built Xyce with correct configurations
    - Lots of diagram building in preparation for our presentation
- Matt Ottersen

    - Got the ADC to pass LVS
    - Started simulating post layout ADC

- Regassa Dukele
    - Got 3-ADC simulation works
    - Works

Pending issues

- How to properly create a layout of ReRAM cell using Magic
- How to simulate the ReRAM device with other components
    - Since all other components have spice netlists, and ReRAM has VerilogA netlist, we will somehow have to merge or convert these netlists for correct simulations

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Simulated ReRAM device and observed switching behavior	6	63
Aiden Petersen	Xyce + Presentation prep	6	56
Matt Ottersen	ADC LVS and Post-Layout Simulation	6	56
Regassa Dukele	ADC simulation and layout	7	57

Plans for the upcoming week

- Joshua Thater
    - Figure out how to simulate ReRAM with other devices
    - Simulate ReRAM with other devices and try to figure out how much current will accumulate on columns of the ReRAM crossbar
- Aiden Petersen
    - Run simulations with xyce
- Matt Ottersen
    - Getting Post-Layout ADC simulation to works as expected
- Regassa Dukele
    - Making ADC layout and works on post layout simulation